

ACKNOWLEDGEMENT RECEIPT

Electronic Version 1.1

Stylesheet Version v1.1.1

Title of Invention	A METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR GENERATING AND VERIFYING ISOLATION LOGIC MODULES IN DESIGN OF INTEGRATED CIRCUITS
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Submission Type : Utility Patent Filing

Application Number:

10/711493



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First Named Applicant: Bhanu KAPOOR

Attorney Docket Number: Q82851

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File Listing:

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us-fee-sheet	us-fee-sheet.xls	24912	2004-09-21
us-fee-sheet	us-fee-sheet.dtd	11069	2004-09-21
us-ids	Q82851-usidst.xml	1350	2004-09-21
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us-ids	us-ids.xls	12026	2004-09-21
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us-assignment	Q82851-usassn.xml	1962	2004-09-21
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us-assignment	Q82851tsg.tif	74188	2004-09-21
us-declaration	Q82851dec1.tif	97550	2004-09-21
us-declaration	Q82851dec2.tif	54862	2004-09-21
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application-body	image6.tif	179275	2004-09-21

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application-body	mmlalias.ent	38209	2004-09-21
application-body	mmlextra.ent	7901	2004-09-21
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application-body	wipo.ent	4956	2004-09-21
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claims-pdf	ABX1-clsms.pdf	48971	2004-09-21
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